METHOD FOR PRINTED CIRCUIT BOARD PANELIZATION

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ABSTRACT OF THE INVENTION

A method for panel optimization provides for optimal layout of printed circuit boards (302-306) on factory arrays (104), as well as the layout of arrays on panels
10 (102). By using nesting algorithms to quickly simulate a large number of permutations, an optimal panelization solution can be quickly reached. The method includes the steps of collecting the necessary data (402), performing a panel dimension loop, an array length loop, and an array width loop. For every case, a total efficiency factor is calculated (422) to help determine the optimal layout.